Amendments to the Claims

The following listing of claims replaces all prior versions and listing of claims in this application:

1-28. (Withdrawn).

29. (Original) A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of transistors, the method comprising:

evaluating whether a first transistor or group of transistors is used for a design implemented in the programmable logic device;

if the first transistor or group of transistors is not used for the design, evaluating a second transistor or group of transistors;

if the first transistor or group of transistors is used for the design, determining whether the first transistor or group of transistors can be reverse biased to operate in a low power mode; and

if the first transistor or group of transistors can be reverse biased to operate in a low power mode and a programmable logic device speed specification and a programmable logic device routability specification permit, reverse biasing the first transistor or group of transistors to operate in low power mode.

30. (Original) The method of claim 29, wherein the evaluating occurs during a synthesis period relating to the first transistor or group of transistors.

31. (Original) The method of claim 29, wherein the evaluating occurs during a routing period relating to the first transistor or group of transistors.

32. (Original) The method of claim 29, wherein the evaluating occurs following a routing period relating to the first transistor or group of transistors.

33. (Original) The method of claim 29, wherein the evaluating occurs during a placement period relating to the first transistor or group of transistors.

34. (Original) The method of claim 29, further comprising determining the change in speed of a function associated with the first transistor or group of transistors, the change in speed that is attributable to the reverse biasing.

35. (Original) The method of claim 29, further comprising reverse biasing all transistors in a programmable logic device region.

36. (Original) The method of claim 29, further comprising reverse biasing all transistors in a programming element.

37. (Original) The method of claim 29, further comprising dynamically reverse biasing a plurality of transistors based on signals received via an input pin.

38. (Original) The method of claim 29, further comprising utilizing at least one of synthesis programming, logic placement programming and routing programming to over-achieve timing goals in a portion of the programmable logic device in order to allow at least one transistor to be reverse biased while still meeting performance requirements for the programmable logic device.

39. (Currently amended) The method of claim 29 further comprising grouping a plurality of signal ~~routs~~ routes into a region of the programmable logic device, the plurality of signal ~~routs~~ routes comprising transistors that may be reverse biased while maintaining the programmable logic device speed specification and the programmable logic device routability specification.

40-55. (Withdrawn)

56. (Original) A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of transistors, the method comprising:

evaluating whether a first transistor is used for a design implemented in the programmable logic device;

if the first transistor is not used for the design, evaluating a second transistor;

if the first transistor is used for the design, determining whether the first transistor can be reverse biased to operate in a low power mode; and

if the first transistor can be reverse biased to operate in a low power mode and a programmable logic device speed specification and a programmable logic device routability specification permit, reverse biasing the first transistor to operate in low power mode.

57-80. (Withdrawn).

81. (Currently amended) A programmable logic device comprising:

a plurality of ~~sub-regions~~ transistors, a first sub-plurality of said transistors being used for a design implemented in the programmable logic device, and

a second sub-plurality of said transistors not being used for said design; and

~~wherein a portion of the transistors in each region is adapted to be reverse-biased during configuration~~ means for reverse-biasing at least some of the transistors in the second sub-plurality in order to reduce leakage current.

82. (Currently amended) The device of claim 81, wherein ~~a portion of the transistors in each region is adapted to be reverse-biased~~ the means for reverse-biasing is at least partly dynamically operable during programmable logic device operation.

83. (Currently amended) The device of claim 81, ~~wherein a portion of the transistors in each region is adapted to be forward biased~~ further comprising:

means for forward biasing at least some of said transistors that are not being reverse biased by the means for reverse biasing in order to speed up the operation of the ~~portion of~~ transistors that are forward biased.

84. (Currently amended) The device of claim 81 wherein the ~~a portion of the transistors in each region is adapted to be forward biased~~ means for forward biasing is at least partly operable during operation of the programmable logic device.

85-95. (Withdrawn).